Pease cancel the claim 4

Claim 5:

Pease cancel the claim 5

In claim 8:

VW 3/23/07 On line 6, after the word "the secondary memory" on page 3, replace a period symbol "." with a semicolon---;--- and insert new lines as follow

---wherein the clock control logic comprises---

---a phase adjuster;---

---cycle control logic coupled to the phase adjuster; and---

---step pulse generator logic coupled to the cycle control logic, and wherein the phase adjuster comprises

a set of delay cells to alter the phase of a primary clock signal.---

Claim 10:

Pease cancel the claim 10

Claim 11:

Pease cancel the claim 11

In claim 12:

On line 2, after the word "the secondary memory" on page 4, replace a period symbol "." with a semicolon---;--- and insert new lines as follow

---wherein the clock control logic comprises---

---a phase adjuster;---

---cycle control logic coupled to the phase adjuster; and---